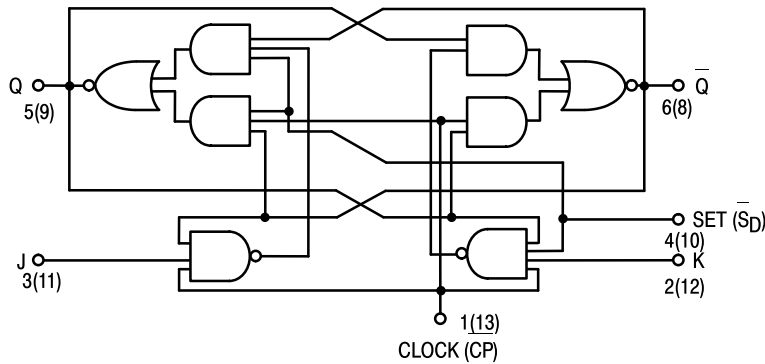




# DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

The SN54/74LS113A offers individual J, K, set, and clock inputs. These monolithic dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum setup times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

LOGIC DIAGRAM (Each Flip-Flop)



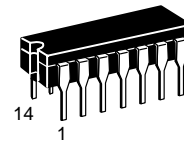
MODE SELECT — TRUTH TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	S <sub>D</sub>	J	K	Q	Q̄
Set	L	X	X	H	L
Toggle	H	h	h	q	q
Load "0" (Reset)	H	l	h	L	H
Load "1" (Set)	H	h	l	H	L
Hold	H	l	l	q	q

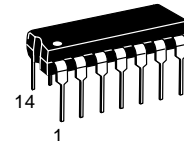
H, h = HIGH Voltage Level  
 L, l = LOW Voltage Level  
 X = Don't Care  
 l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

## SN54/74LS113A

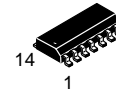
DUAL JK NEGATIVE  
 EDGE-TRIGGERED FLIP-FLOP  
 LOW POWER SCHOTTKY



J SUFFIX  
 CERAMIC  
 CASE 632-08



N SUFFIX  
 PLASTIC  
 CASE 646-06

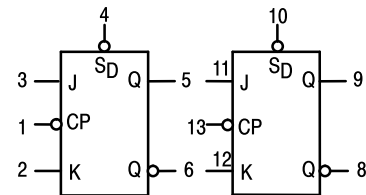


D SUFFIX  
 SOIC  
 CASE 751A-02

ORDERING INFORMATION

- SN54LSXXXJ Ceramic
- SN74LSXXXN Plastic
- SN74LSXXXD SOIC

LOGIC SYMBOL



V<sub>CC</sub> = PIN 14  
 GND = PIN 7

# SN54/74LS113A

## GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T <sub>A</sub>	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I <sub>OH</sub>	Output Current — High	54, 74			-0.4	mA
I <sub>OL</sub>	Output Current — Low	54 74			4.0 8.0	mA

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V <sub>IL</sub>	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA	
V <sub>OH</sub>	Output HIGH Voltage	54	2.5	3.5	V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table	
		74	2.7	3.5	V		
V <sub>OL</sub>	Output LOW Voltage	54, 74		0.25	0.4	V	I <sub>OL</sub> = 4.0 mA V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
		74		0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current	J, K Set Clock			20 60 80	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
		J, K Set Clock			0.1 0.3 0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current	J, K Set, Clock			-0.4 -0.8	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>OS</sub>	Short Circuit Current (Note 1)		-20		-100	mA	V <sub>CC</sub> = MAX
I <sub>CC</sub>	Power Supply Current				6.0	mA	V <sub>CC</sub> = MAX

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

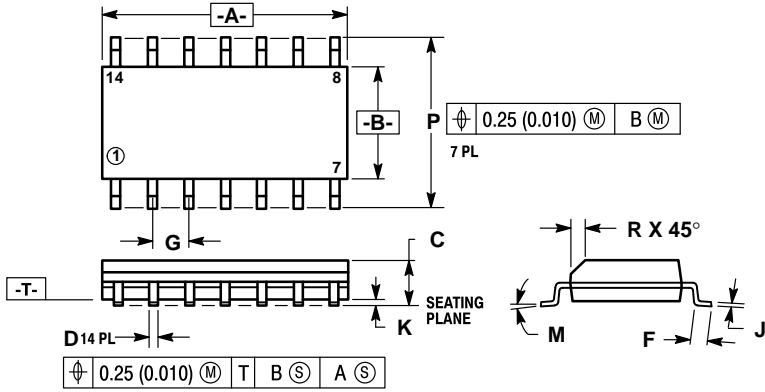
## AC CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
f <sub>MAX</sub>	Maximum Clock Frequency	30	45		MHz	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PLH</sub>	Propagation Delay, Clock Set to Output		15	20	ns	
t <sub>PHL</sub>			15	20	ns	

## AC SETUP REQUIREMENTS (T<sub>A</sub> = 25°C, V<sub>CC</sub> = 5.0 V)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>W</sub>	Clock Pulse Width High	20			ns	V <sub>CC</sub> = 5.0 V
t <sub>W</sub>	Set Pulse Width	25			ns	
t <sub>s</sub>	Setup Time	20			ns	
t <sub>h</sub>	Hold Time	0			ns	

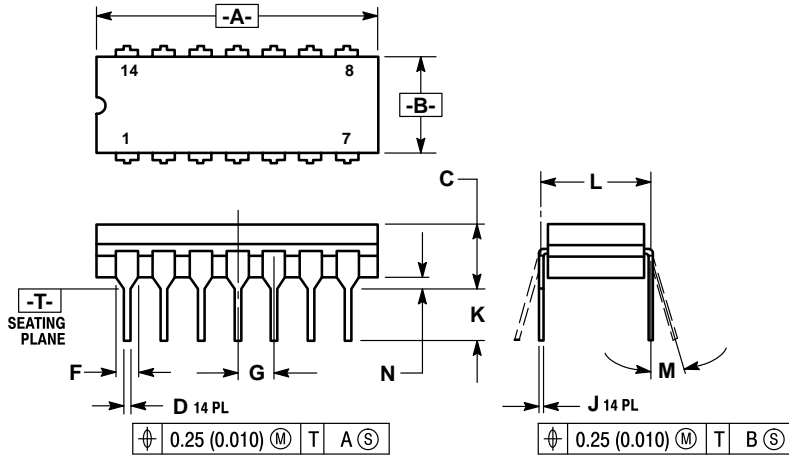
**Case 751A-02 D Suffix  
14-Pin Plastic  
SO-14**



- NOTES:
1. DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
  2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  3. CONTROLLING DIMENSION: MILLIMETER.
  4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
  5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  6. 751A-01 IS OBSOLETE, NEW STANDARD 751A-02.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

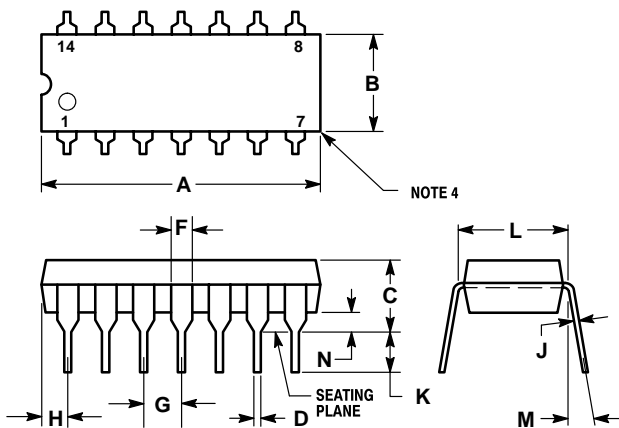
**Case 632-08 J Suffix  
14-Pin Ceramic Dual In-Line**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.
  5. 632-01 THRU -07 OBSOLETE, NEW STANDARD 632-08.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.39	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

**Case 646-06 N Suffix  
14-Pin Plastic**



- NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
  2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
  3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
  4. ROUNDED CORNERS OPTIONAL.
  5. 646-05 OBSOLETE, NEW STANDARD 646-06.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.39	1.01	0.015	0.039